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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,171	07/09/2003	Evgueniy Nikolov Stefanov	ONS00393	7154
7590	12/30/2004		EXAMINER	
James J. Stipanuk Semiconductor Components Industries, L.L.C. Patent Administration Dept - MD/A700 P.O. Box 62890 Phoenix, AZ 85082-2890			WARREN, MATTHEW E	
			ART UNIT	PAPER NUMBER
			2815	
			DATE MAILED: 12/30/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/615,171	STEFANOV ET AL.
	Examiner	Art Unit
	Matthew E Warren	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 12 October 2004.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-9 and 11-15 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-9 and 11-15 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____

DETAILED ACTION

This Office Action is in response to the Amendment filed on October 12, 2004.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, 6, 7, 9-11, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (US 6,365,924 B1) in view of Mori (US 4,246,594).

In re claim 1, Wang et al. shows (fig. 3) a high frequency integrated circuit structure comprising: internal circuitry formed in a first active region (col. 1, lines 24-30); and a second active region comprising a first semiconductor layer (116) of the second conductivity type (N) formed over a substrate. A first silicon controlled rectifier device is formed in the second active region, the first silicon controlled rectifier device comprising a first well region (118) of the first conductivity type (P) formed in the semiconductor layer (116), a first doped region (124) of the first conductivity type (P) formed in the first well region, a second well region (114) of the first conductivity type (P) formed in the first semiconductor layer (116) and spaced apart from the first well region. A second doped region (112) of the second conductivity type (N) is also formed in the second well region. A second silicon controlled rectifier device comprises the second well region

(114), a third doped region (122) of the first conductivity type (P) formed in the second well region, the first well region (118), and a fourth doped region (120) of the second conductivity type (N), wherein the first and second silicon controlled rectifier devices are coupled to the internal circuitry and form an ESD structure for protecting the internal circuitry against positive and negative ESD stresses (col. 4, lines 17-28). Wang shows all of the elements of the claims except the body of semiconductor material comprising a first conductivity type and the buried layer of the second conductivity type formed over the body of semiconductor material. Mori shows (fig. 3a) a high speed switching device having a first doped region of a first conductivity type (P+ substrate 24), a body of semiconductor material of the first conductivity type (P layer 26), and a buried region of the second conductivity type (N+ buried layer 12₂). A first semiconductor layer (14₂) of the second conductivity type (N) is formed over the buried layer, wherein the first semiconductor layer has a lower dopant concentration (N) than the buried layer (N+). With such a configuration, the substrate capacitance is lowered and the withstand voltage is increased (col. 4, lines 25-49). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the SCR protection structure of Wang by adding a first well region of the first conductivity type to the substrate as taught by Mori to lower the substrate capacitance and increase the withstand voltage.

In re claim 2, Mori shows (fig. 3a) that the body of semiconductor material comprises a semiconductor wafer having the first conductivity type (P+ substrate 24), and a second semiconductor layer (26) formed over the semiconductor wafer, wherein

the second semiconductor layer comprises the first conductivity type (P layer 26), wherein the first semiconductor layer has a lower dopant concentration (P) than the semiconductor wafer (P+).

In re claim 3, Wang et al. shows (fig. 3) that a first ohmic contact (K) couples the first and fourth doped regions and that a second ohmic contact (A) couples the second and third doped regions.

In re claim 4, Mori shows (fig. 3a) deep isolation or deep contact trenches (28) extending from a surface of the first semiconductor layer into the substrate to form isolation for the switching or thyristor devices (S22 and S13).

In re claims 6 and 7, the references do not show that the first semiconductor layer has a dopant concentration of approximately 1.0×10^{13} atoms/cm³ or that the semiconductor layer has a thickness from about 1.5 microns to about 3.0 microns. However, It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the semiconductor layer having the specified doping concentration or thickness, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

In re claim 9, Wang et al. shows (fig. 3) a symmetrical SCR device comprising: a semiconductor substrate (P substrate) of a first conductive type (P); a second semiconductor layer (116) of a second conductivity type (N) formed adjacent the substrate. First and second wells (P base) comprising a first conductivity type formed in

the semiconductor layer, wherein the first and second wells are spaced apart. First and second doped regions (124 and 120) are formed in the first well, wherein the first doped region comprises the first conductivity type and the second doped region comprises the second conductivity type. The first and second doped regions are electrically coupled by contact K. Third and fourth doped regions (112 and 122) are formed in the second well, wherein the third doped region comprises the first conductivity type and the fourth doped region comprises the second conductivity type. The third and fourth doped regions are electrically coupled contact A. Wang shows all of the elements of the claims except a second semiconductor layer of the first conductivity type formed over the first semiconductor layer, wherein the second semiconductor layer has a lower dopant concentration than the first semiconductor layer. Mori shows (fig. 3a) a high speed switching device having a semiconductor substrate of the first conductivity type (P+ substrate 24), a first semiconductor layer of the first conductivity type (P layer 26) formed over the semiconductor substrate, wherein the first semiconductor layer has a lower dopant concentration than the semiconductor substrate. A second semiconductor layer (12₂) of the second conductivity type (N+ buried layer 12₂) is formed adjacent the first semiconductor layer and a third semiconductor layer (N layer 14) of the second conductivity type is formed adjacent the second semiconductor layer, wherein the second semiconductor layer has a lower dopant concentration than the first semiconductor layer. With such a configuration, the substrate capacitance is lowered and the withstand voltage is increased (col. 4, lines 25-49). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to

modify the SCR protection structure of Wang by adding a second semiconductor layer of the first conductivity type to the substrate as taught by Mori to lower the substrate capacitance and increase the withstand voltage.

In re claim 11, the references do not show that the first semiconductor layer has a dopant concentration of approximately 1.0×10^{13} atoms/cm³ or that the semiconductor layer has a thickness from about 1.5 microns to about 3.0 microns. However, It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the semiconductor layer having the specified doping concentration or thickness, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

In re claim 15, Wang shows (fig. 3) that the first conductivity type is p-type and the second conductivity type is n-type.

Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (US 6,365,924 B1) in view of Mori (US 4,246,594) as applied to claims 1 and 9 above, and further in view of Duvvury et al. (US 6,365,940 B1).

In re claims 5 and 14, neither Wang nor Mori show a field dielectric region between first and second wells, which Duvvury et al. shows in figure 2 (FOX regions 236) to provide isolation between the wells. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the SCR of

Wang and Mori by providing field dielectric regions as taught by Duvvury to provide isolation between wells.

Claims 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (US 6,365,924 B1) in view of Mori (US 4,246,594) as applied to claims 1 and 9 above, and further in view of Pavier et al. (US Pub. 2003/0062622 A1)

In re claims 8 and 12, Wang in view Mori shows all of the elements of the claims except the deep isolation trench including a dielectric layer extending into the substrate. Pavier et al. shows (fig. 2) a semiconductor device having an isolation trench (70) of oxide extending into a substrate (31) from the top surface of a semiconductor layer (32) to separate various devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the isolation zones of Wang and Mori by forming deep isolation trenches of dielectric as taught by Pavier to separate various devices formed on a substrate.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (US 6,365,924 B1) in view of Mori (US 4,246,594) as applied to claim 9 above, and further in view of Norstrom et al. (US 6,610,578 B2)

In re claim 13, Wang in view Mori shows all of the elements of the claims except the deep contact trench extending into the substrate. Norstrom et al. shows (fig. 34b) a semiconductor device having contact trench (85) extending into a substrate (1) from the top surface of a semiconductor layer to provide a connection to the substrate.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined SCR of Wang and Mori by forming deep contact trenches as taught by Norstrom to provide a contact to the substrate.

Response to Arguments

Applicant's arguments filed with respect to claims 1-15 have been fully considered but they are not persuasive. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, although Wang teaches a dual direction SCR and Mori teaches a unidirectional bipolar SCR switch, both references still teach an SCR device. For that reason, the components of one SCR device can be applied to another. Mori discloses a device having a buried layer and additional substrate layers formed on a substrate to ultimately increase the withstand voltage of the device. Someone of ordinary skill in the art desiring to increase the withstand voltage of a semiconductor device would look to Mori for this teaching. Although the applicant uses the various layers for different reasons, one cannot overlook the teachings of Mori. The applicant has merely found

additional benefits of such a combination. For these reasons, the cited references show all of the elements of the claims and this action is made final.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2815

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW

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December 27, 2004

Tom Thomas
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